FIG.1

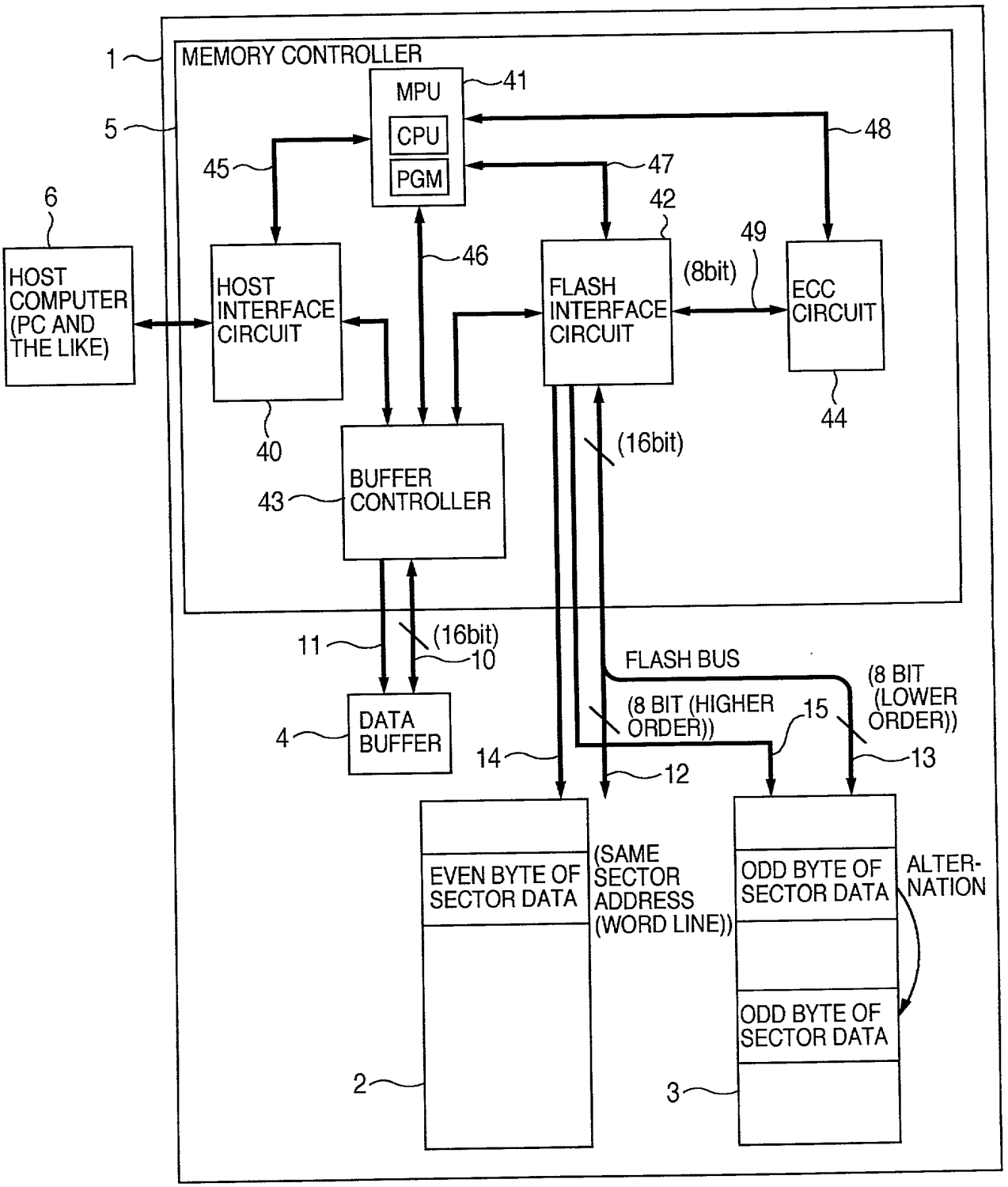
1
MEMORY CONTROLLER
MPU
41
CPU
PGM
5
45
47
48
42
6
46
49
HOST COMPUTER (PC AND THE LIKE)
HOST INTERFACE CIRCUIT
FLASH INTERFACE CIRCUIT
(8bit)
ECC CIRCUIT
40
44
(16bit)
43
BUFFER CONTROLLER
11
(16bit)
10
FLASH BUS
(8 BIT (LOWER ORDER))
(8 BIT (HIGHER ORDER))
15
4
DATA BUFFER
14
13
12
EVEN BYTE OF SECTOR DATA
(SAME SECTOR ADDRESS (WORD LINE))
ODD BYTE OF SECTOR DATA
ALTER-NATION
ODD BYTE OF SECTOR DATA
2
3

FIG.2

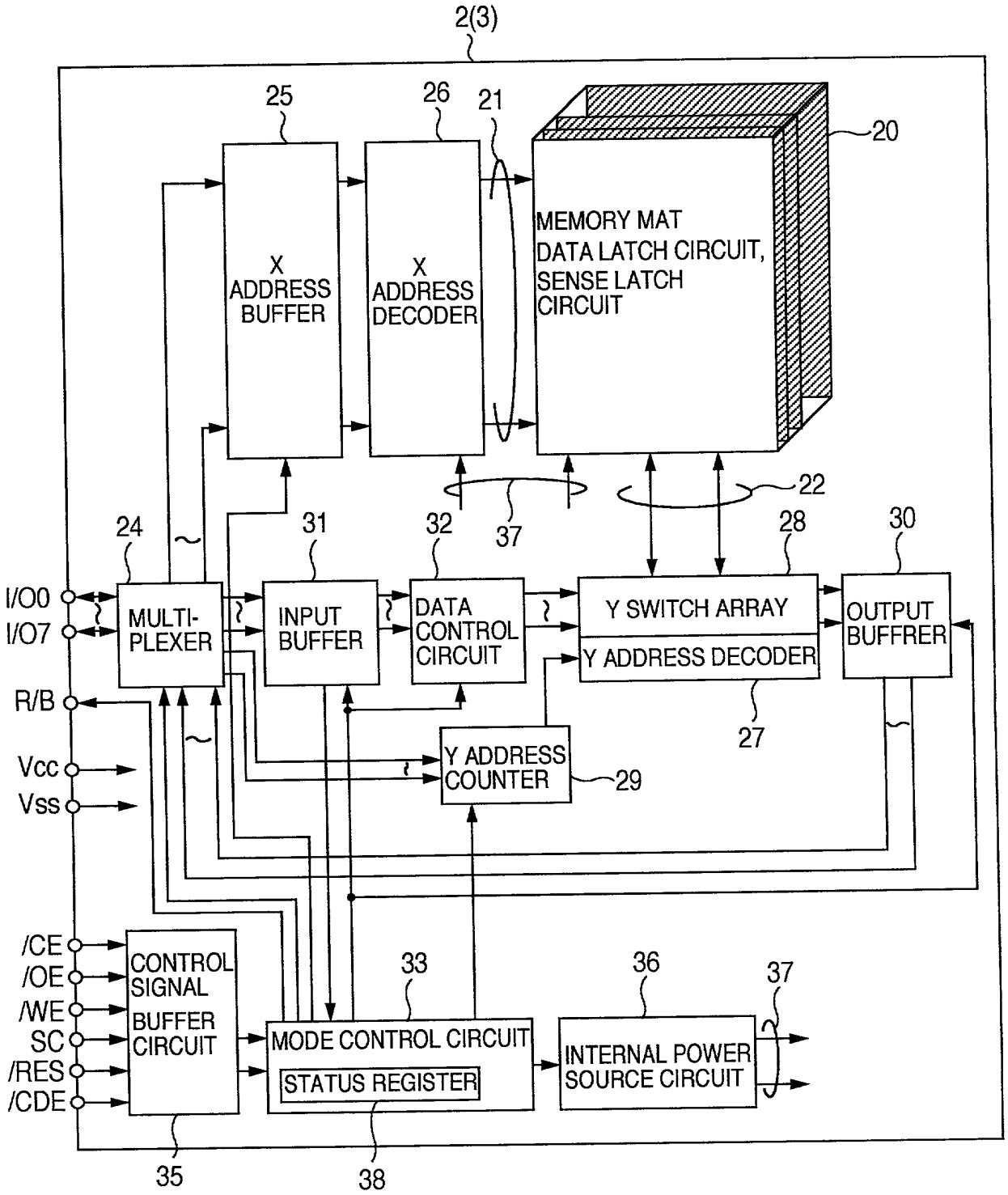
2(3)
25
26
21
20
X ADDRESS BUFFER
X ADDRESS DECODER
MEMORY MAT
DATA LATCH CIRCUIT, SENSE LATCH CIRCUIT
22
37
24
31
32
28
30
I/O0
I/O7
MULTI-PLEXER
INPUT BUFFER
DATA CONTROL CIRCUIT
Y SWITCH ARRAY
Y ADDRESS DECODER
OUTPUT BUFFRER
27
R/B
Vcc
Vss
Y ADDRESS COUNTER
29
/CE
/OE
/WE
SC
/RES
/CDE
CONTROL SIGNAL BUFFER CIRCUIT
33
36
37
MODE CONTROL CIRCUIT
STATUS REGISTER
INTERNAL POWER SOURCE CIRCUIT
35
38

FIG.3

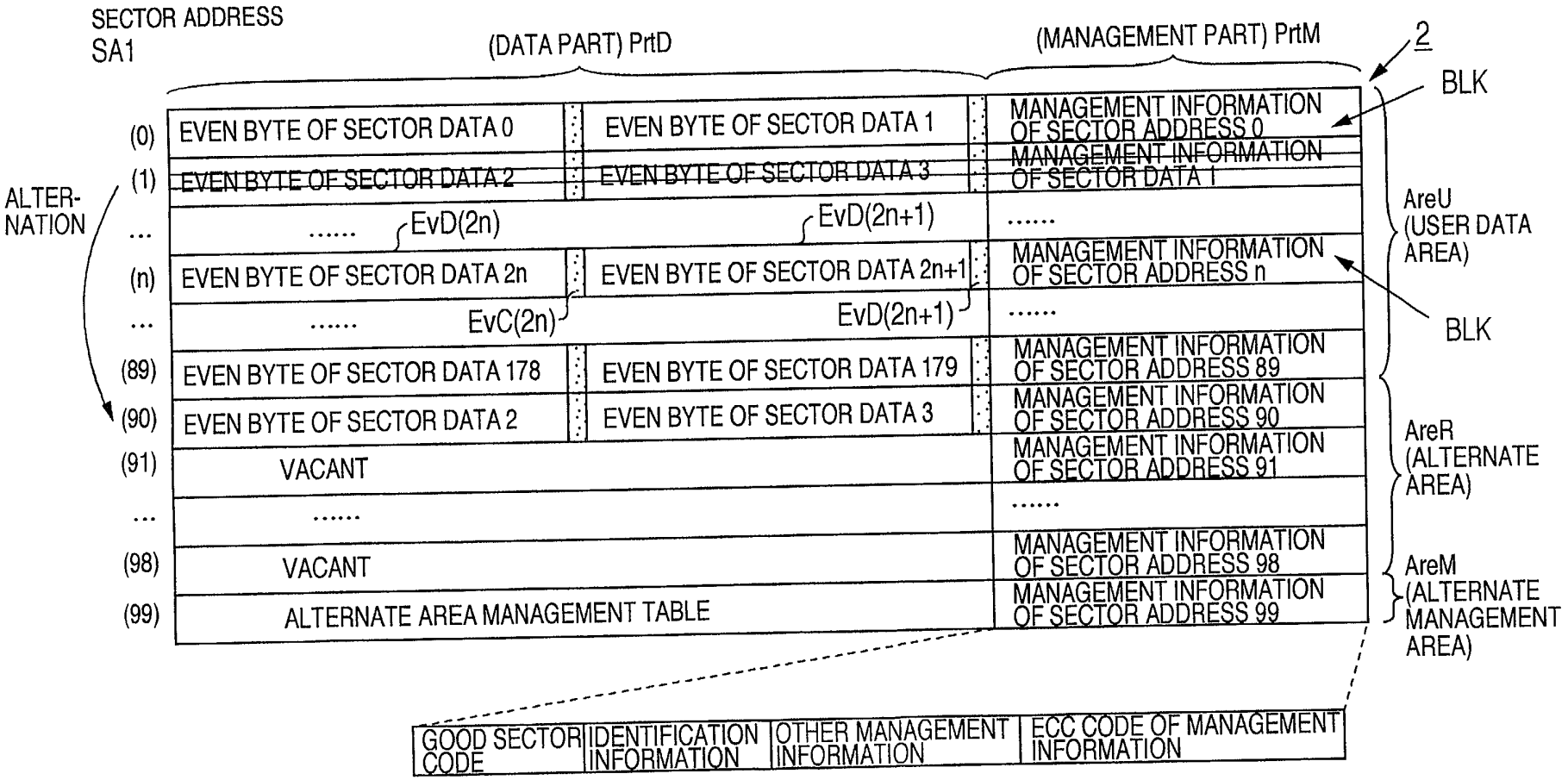
SECTOR ADDRESS
SA1
(DATA PART) PrtD
(MANAGEMENT PART) PrtM
2
BLK
ALTER-
NATION
(0)
EVEN BYTE OF SECTOR DATA 0
EVEN BYTE OF SECTOR DATA 1
MANAGEMENT INFORMATION OF SECTOR ADDRESS 0
(1)
EVEN BYTE OF SECTOR DATA 2
EVEN BYTE OF SECTOR DATA 3
MANAGEMENT INFORMATION OF SECTOR DATA 1
...
EvD(2n)
EvD(2n+1)
(n)
EVEN BYTE OF SECTOR DATA 2n
EVEN BYTE OF SECTOR DATA 2n+1
MANAGEMENT INFORMATION OF SECTOR ADDRESS n
EvC(2n)
EvD(2n+1)
BLK
(89)
EVEN BYTE OF SECTOR DATA 178
EVEN BYTE OF SECTOR DATA 179
MANAGEMENT INFORMATION OF SECTOR ADDRESS 89
(90)
EVEN BYTE OF SECTOR DATA 2
EVEN BYTE OF SECTOR DATA 3
MANAGEMENT INFORMATION OF SECTOR ADDRESS 90
(91)
VACANT
MANAGEMENT INFORMATION OF SECTOR ADDRESS 91
(98)
VACANT
MANAGEMENT INFORMATION OF SECTOR ADDRESS 98
(99)
ALTERNATE AREA MANAGEMENT TABLE
MANAGEMENT INFORMATION OF SECTOR ADDRESS 99
AreU (USER DATA AREA)
AreR (ALTERNATE AREA)
AreM (ALTERNATE MANAGEMENT AREA)
GOOD SECTOR CODE
IDENTIFICATION INFORMATION
OTHER MANAGEMENT INFORMATION
ECC CODE OF MANAGEMENT INFORMATION

FIG.4

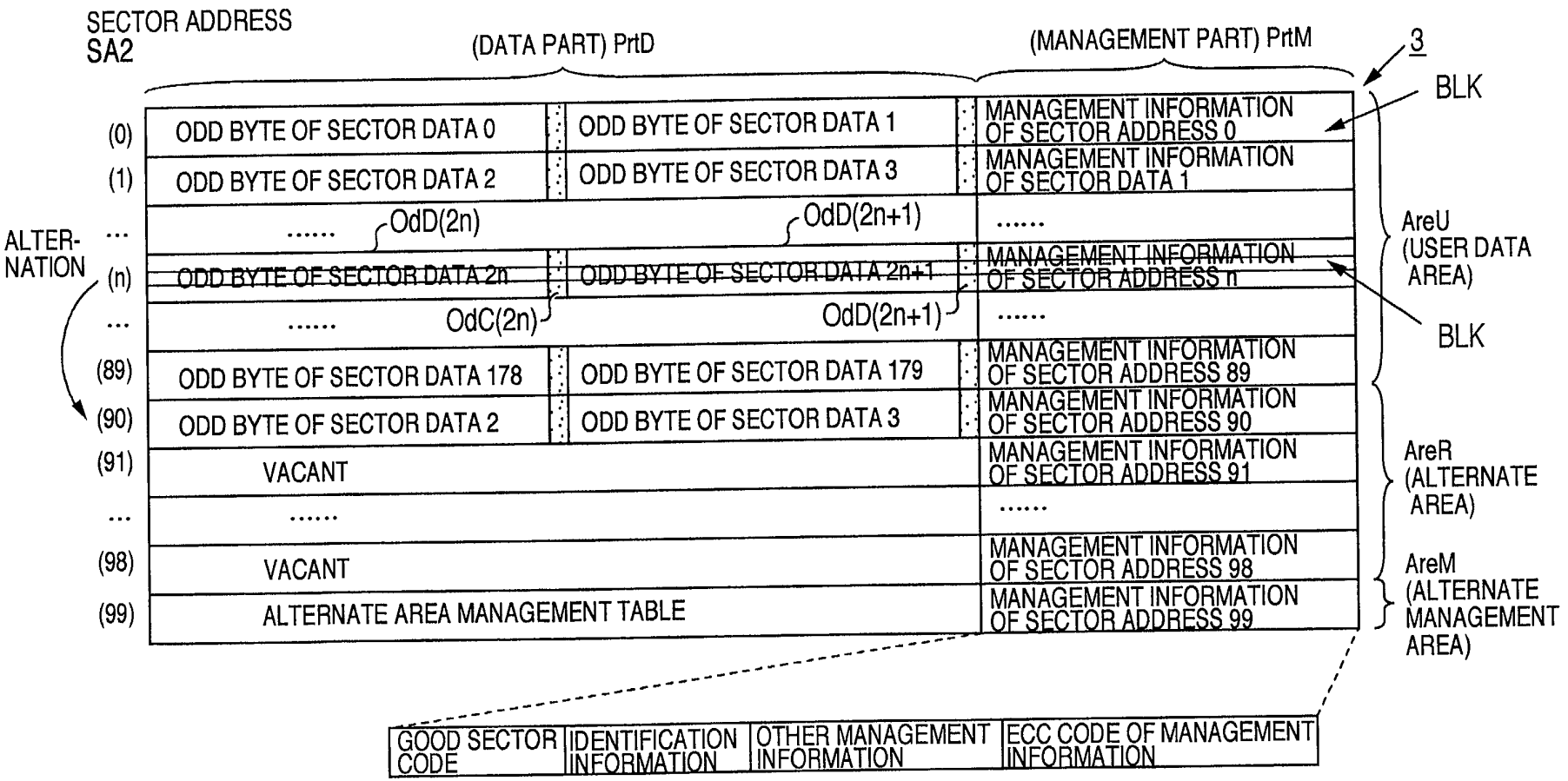
SECTOR ADDRESS
SA2
(DATA PART) PrtD
(MANAGEMENT PART) PrtM
3
BLK
ALTER-
NATION
(0)
(1)
(n)
(89)
(90)
(91)
(98)
(99)
ODD BYTE OF SECTOR DATA 0
ODD BYTE OF SECTOR DATA 1
MANAGEMENT INFORMATION OF SECTOR ADDRESS 0
ODD BYTE OF SECTOR DATA 2
ODD BYTE OF SECTOR DATA 3
MANAGEMENT INFORMATION OF SECTOR DATA 1
OdD(2n)
OdD(2n+1)
ODD BYTE OF SECTOR DATA 2n
ODD BYTE OF SECTOR DATA 2n+1
MANAGEMENT INFORMATION OF SECTOR ADDRESS n
OdC(2n)
OdD(2n+1)
ODD BYTE OF SECTOR DATA 178
ODD BYTE OF SECTOR DATA 179
MANAGEMENT INFORMATION OF SECTOR ADDRESS 89
ODD BYTE OF SECTOR DATA 2
ODD BYTE OF SECTOR DATA 3
MANAGEMENT INFORMATION OF SECTOR ADDRESS 90
VACANT
MANAGEMENT INFORMATION OF SECTOR ADDRESS 91
VACANT
MANAGEMENT INFORMATION OF SECTOR ADDRESS 98
ALTERNATE AREA MANAGEMENT TABLE
MANAGEMENT INFORMATION OF SECTOR ADDRESS 99
AreU (USER DATA AREA)
AreR (ALTERNATE AREA)
AreM (ALTERNATE MANAGEMENT AREA)
GOOD SECTOR CODE
IDENTIFICATION INFORMATION
OTHER MANAGEMENT INFORMATION
ECC CODE OF MANAGEMENT INFORMATION

FIG.5

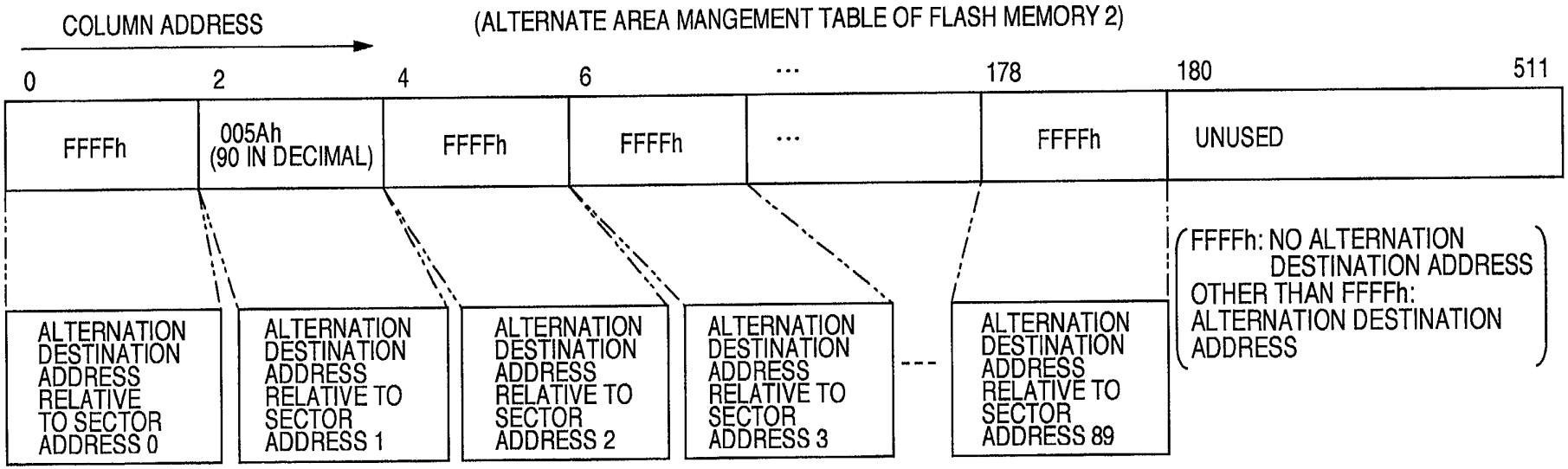
COLUMN ADDRESS
(ALTERNATE AREA MANGEMENT TABLE OF FLASH MEMORY 2)
0
2
4
6
...
178
180
511
FFFFh
005Ah
(90 IN DECIMAL)
FFFFh
FFFFh
...
FFFFh
UNUSED
FFFFh: NO ALTERNATION DESTINATION ADDRESS
OTHER THAN FFFFh: ALTERNATION DESTINATION ADDRESS
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 0
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 1
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 2
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 3
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 89

FIG.6

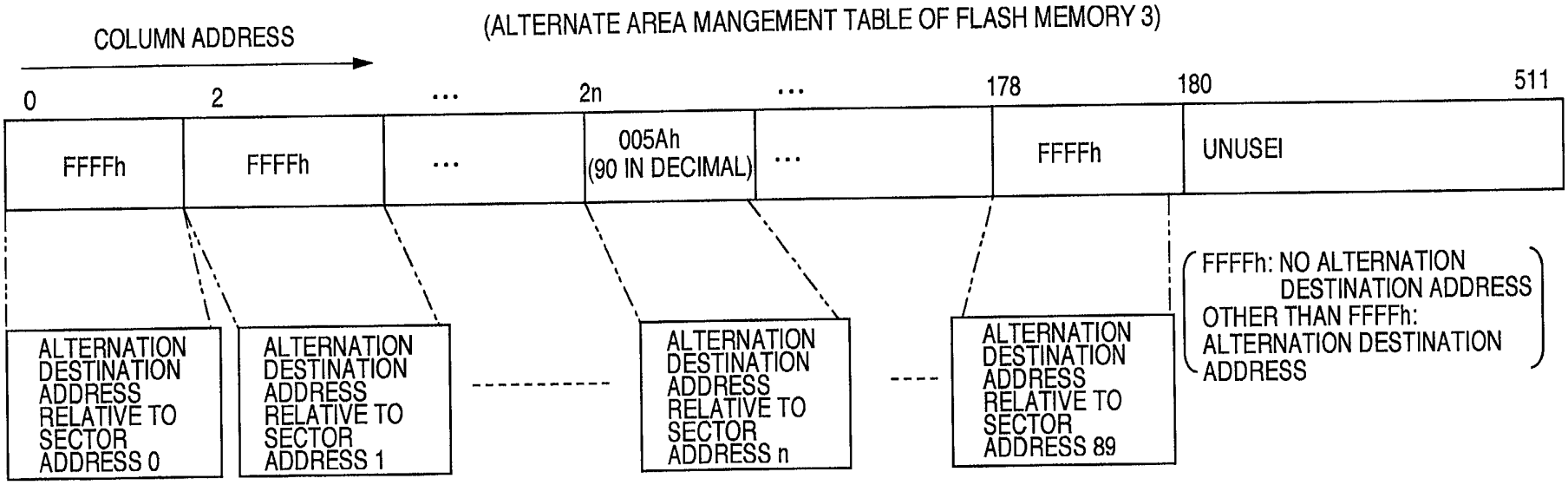
(ALTERNATE AREA MANGEMENT TABLE OF FLASH MEMORY 3)
COLUMN ADDRESS
0
2
2n
178
180
511
FFFFh
FFFFh
005Ah
(90 IN DECIMAL)
FFFFh
UNUSEI
FFFFh: NO ALTERNATION DESTINATION ADDRESS
OTHER THAN FFFFh: ALTERNATION DESTINATION ADDRESS
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 0
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 1
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS n
ALTERNATION DESTINATION ADDRESS RELATIVE TO SECTOR ADDRESS 89

FIG.7

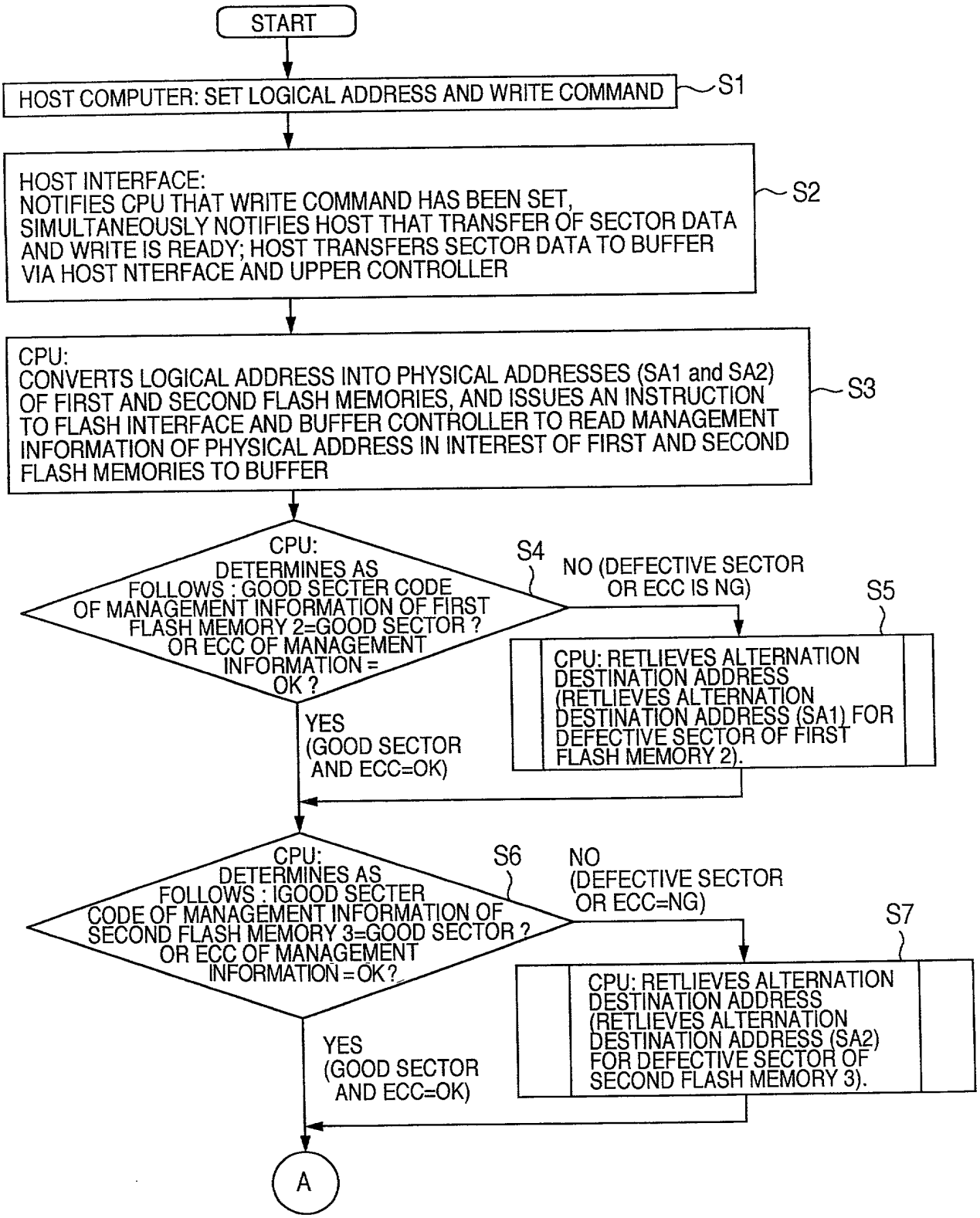
START
HOST COMPUTER: SET LOGICAL ADDRESS AND WRITE COMMAND
S1
HOST INTERFACE:
NOTIFIES CPU THAT WRITE COMMAND HAS BEEN SET,
SIMULTANEOUSLY NOTIFIES HOST THAT TRANSFER OF SECTOR DATA
AND WRITE IS READY; HOST TRANSFERS SECTOR DATA TO BUFFER
VIA HOST NTERFACE AND UPPER CONTROLLER
S2
CPU:
CONVERTS LOGICAL ADDRESS INTO PHYSICAL ADDRESSES (SA1 and SA2)
OF FIRST AND SECOND FLASH MEMORIES, AND ISSUES AN INSTRUCTION
TO FLASH INTERFACE AND BUFFER CONTROLLER TO READ MANAGEMENT
INFORMATION OF PHYSICAL ADDRESS IN INTEREST OF FIRST AND SECOND
FLASH MEMORIES TO BUFFER
S3
CPU:
DETERMINES AS
FOLLOWS : GOOD SECTER CODE
OF MANAGEMENT INFORMATION OF FIRST
FLASH MEMORY 2=GOOD SECTOR ?
OR ECC OF MANAGEMENT
INFORMATION =
OK ?
S4
NO (DEFECTIVE SECTOR
OR ECC IS NG)
S5
CPU: RETLIEVES ALTERNATION
DESTINATION ADDRESS
(RETLIEVES ALTERNATION
DESTINATION ADDRESS (SA1) FOR
DEFECTIVE SECTOR OF FIRST
FLASH MEMORY 2).
YES
(GOOD SECTOR
AND ECC=OK)
CPU:
DETERMINES AS
FOLLOWS : IGOOD SECTER
CODE OF MANAGEMENT INFORMATION OF
SECOND FLASH MEMORY 3=GOOD SECTOR ?
OR ECC OF MANAGEMENT
INFORMATION = OK?
S6
NO
(DEFECTIVE SECTOR
OR ECC=NG)
S7
CPU: RETLIEVES ALTERNATION
DESTINATION ADDRESS
(RETLIEVES ALTERNATION
DESTINATION ADDRESS (SA2)
FOR DEFECTIVE SECTOR OF
SECOND FLASH MEMORY 3).
YES
(GOOD SECTOR
AND ECC=OK)
A

FIG.8

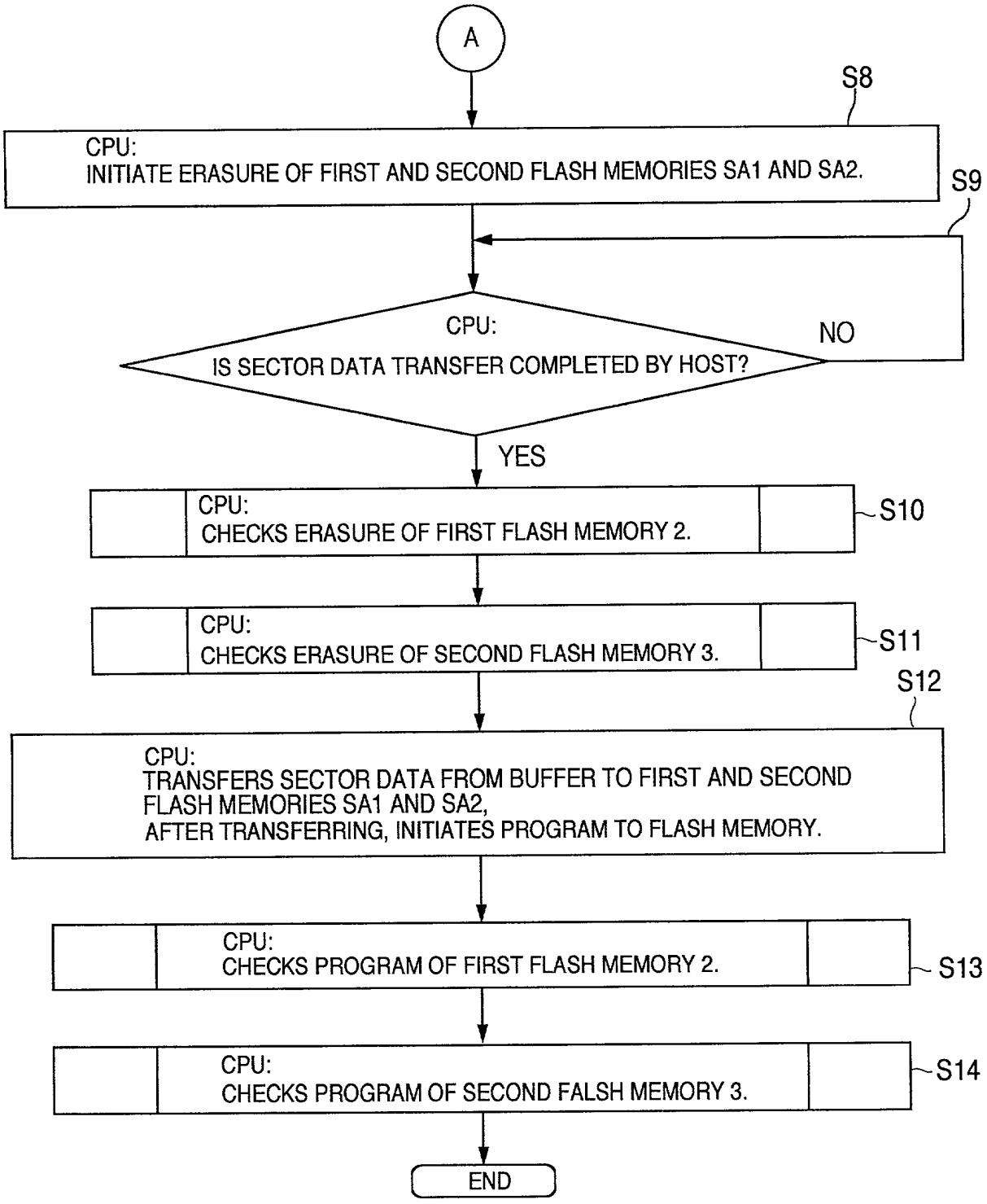
A
S8
CPU:
INITIATE ERASURE OF FIRST AND SECOND FLASH MEMORIES SA1 AND SA2.
S9
CPU:
IS SECTOR DATA TRANSFER COMPLETED BY HOST?
NO
YES
CPU:
CHECKS ERASURE OF FIRST FLASH MEMORY 2.
S10
CPU:
CHECKS ERASURE OF SECOND FLASH MEMORY 3.
S11
S12
CPU:
TRANSFERS SECTOR DATA FROM BUFFER TO FIRST AND SECOND FLASH MEMORIES SA1 AND SA2,
AFTER TRANSFERRING, INITIATES PROGRAM TO FLASH MEMORY.
CPU:
CHECKS PROGRAM OF FIRST FLASH MEMORY 2.
S13
CPU:
CHECKS PROGRAM OF SECOND FALSH MEMORY 3.
S14
END

FIG.9

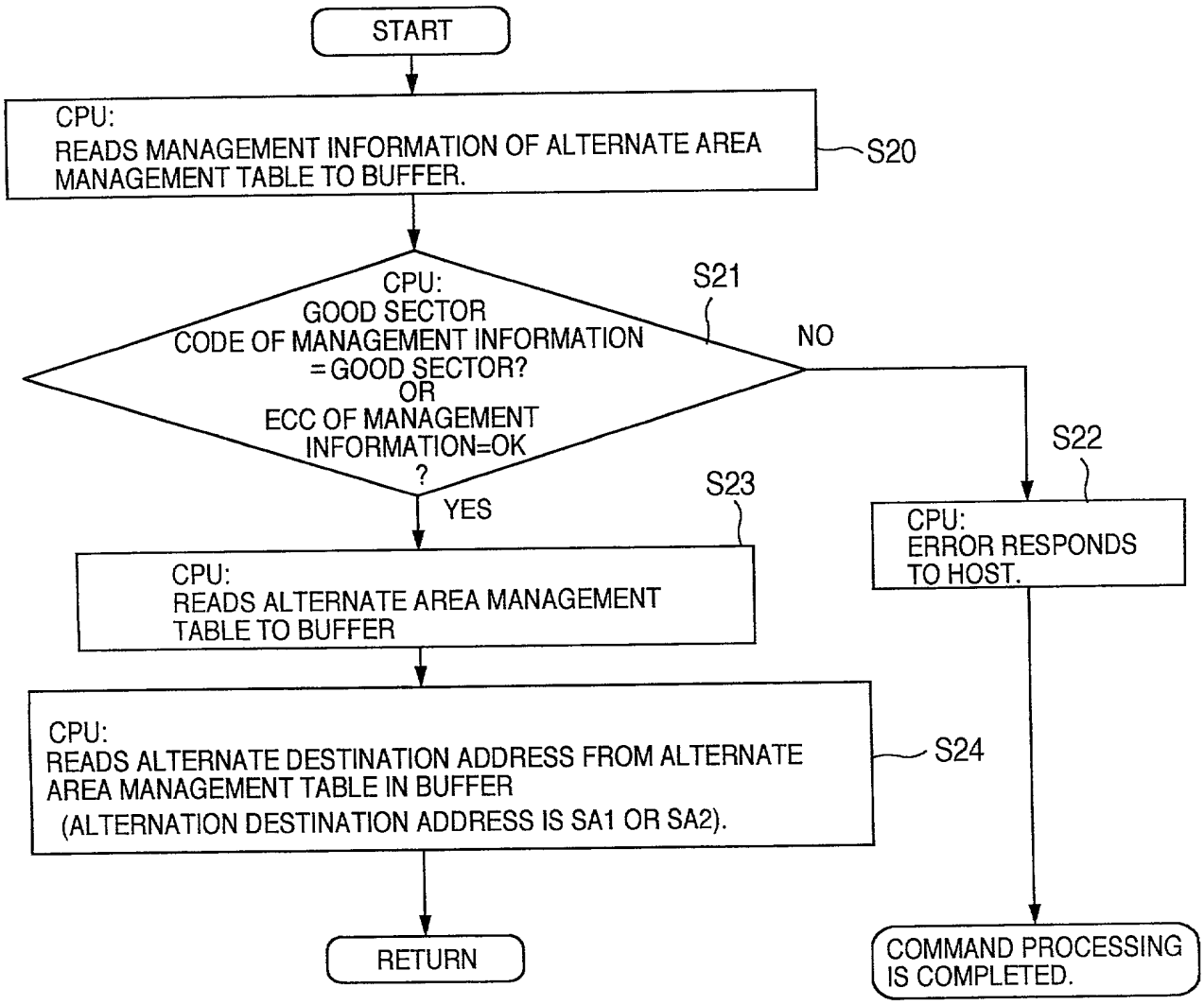
START
CPU:
READS MANAGEMENT INFORMATION OF ALTERNATE AREA MANAGEMENT TABLE TO BUFFER.
S20
CPU:
GOOD SECTOR
CODE OF MANAGEMENT INFORMATION
=GOOD SECTOR?
OR
ECC OF MANAGEMENT
INFORMATION=OK
?
S21
NO
YES
S22
CPU:
ERROR RESPONDS TO HOST.
S23
CPU:
READS ALTERNATE AREA MANAGEMENT TABLE TO BUFFER
CPU:
READS ALTERNATE DESTINATION ADDRESS FROM ALTERNATE AREA MANAGEMENT TABLE IN BUFFER
(ALTERNATION DESTINATION ADDRESS IS SA1 OR SA2).
S24
RETURN
COMMAND PROCESSING IS COMPLETED.

FIG.10

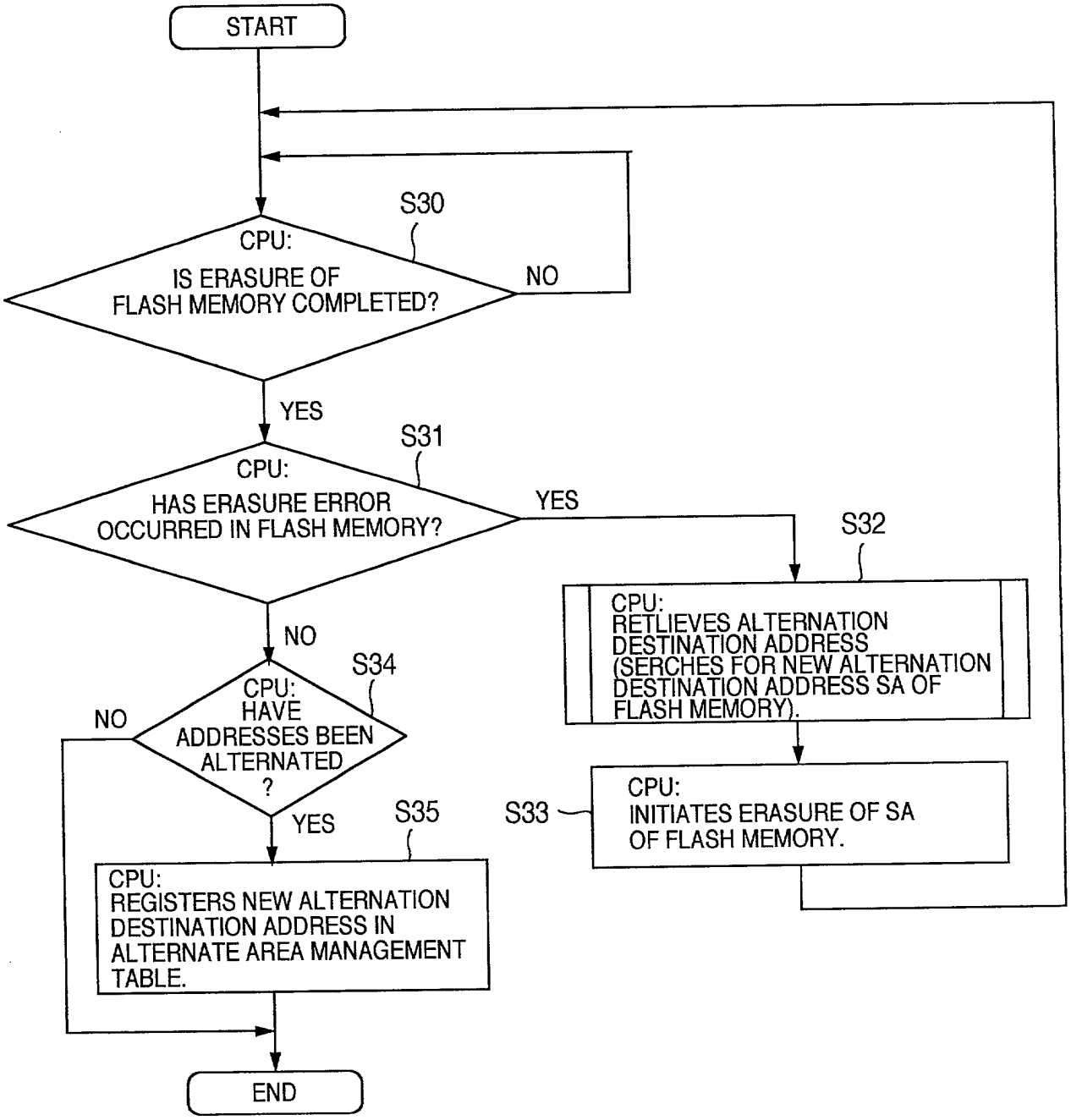
START
S30
CPU:
IS ERASURE OF FLASH MEMORY COMPLETED?
NO
YES
S31
CPU:
HAS ERASURE ERROR OCCURRED IN FLASH MEMORY?
YES
S32
CPU:
RETLIEVES ALTERNATION DESTINATION ADDRESS (SERCHES FOR NEW ALTERNATION DESTINATION ADDRESS SA OF FLASH MEMORY).
S33
CPU:
INITIATES ERASURE OF SA OF FLASH MEMORY.
NO
S34
CPU:
HAVE ADDRESSES BEEN ALTERNATED ?
NO
YES
S35
CPU:
REGISTERS NEW ALTERNATION DESTINATION ADDRESS IN ALTERNATE AREA MANAGEMENT TABLE.
END

FIG.11

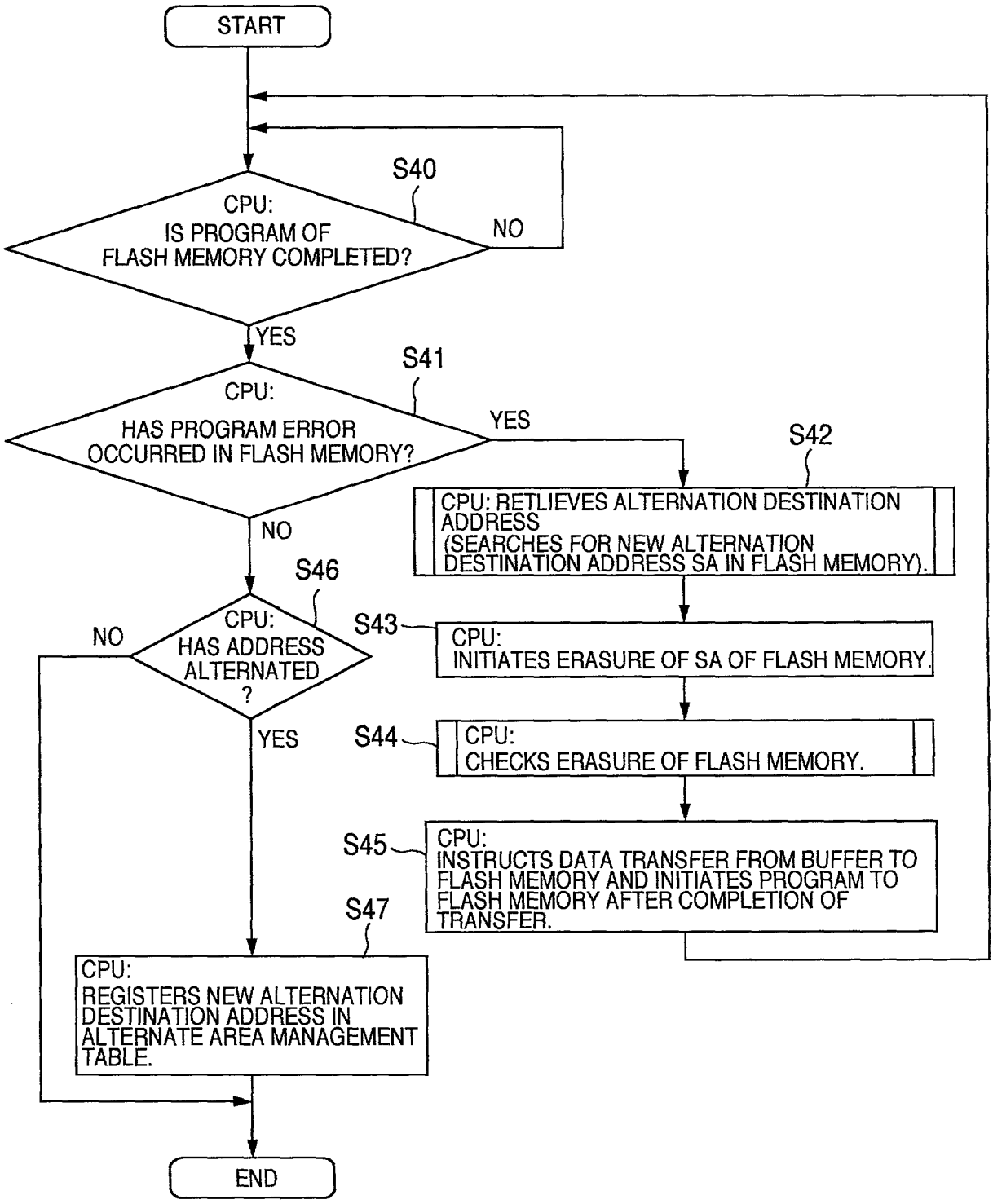
START
S40
CPU:
IS PROGRAM OF
FLASH MEMORY COMPLETED?
NO
YES
S41
CPU:
HAS PROGRAM ERROR
OCCURRED IN FLASH MEMORY?
YES
NO
S42
CPU: RETLIEVES ALTERNATION DESTINATION ADDRESS
(SEARCHES FOR NEW ALTERNATION DESTINATION ADDRESS SA IN FLASH MEMORY).
S43
CPU:
INITIATES ERASURE OF SA OF FLASH MEMORY.
S44
CPU:
CHECKS ERASURE OF FLASH MEMORY.
S45
CPU:
INSTRUCTS DATA TRANSFER FROM BUFFER TO FLASH MEMORY AND INITIATES PROGRAM TO FLASH MEMORY AFTER COMPLETION OF TRANSFER.
S46
CPU:
HAS ADDRESS
ALTERNATED
?
NO
YES
S47
CPU:
REGISTERS NEW ALTERNATION DESTINATION ADDRESS IN ALTERNATE AREA MANAGEMENT TABLE.
END

FIG.12

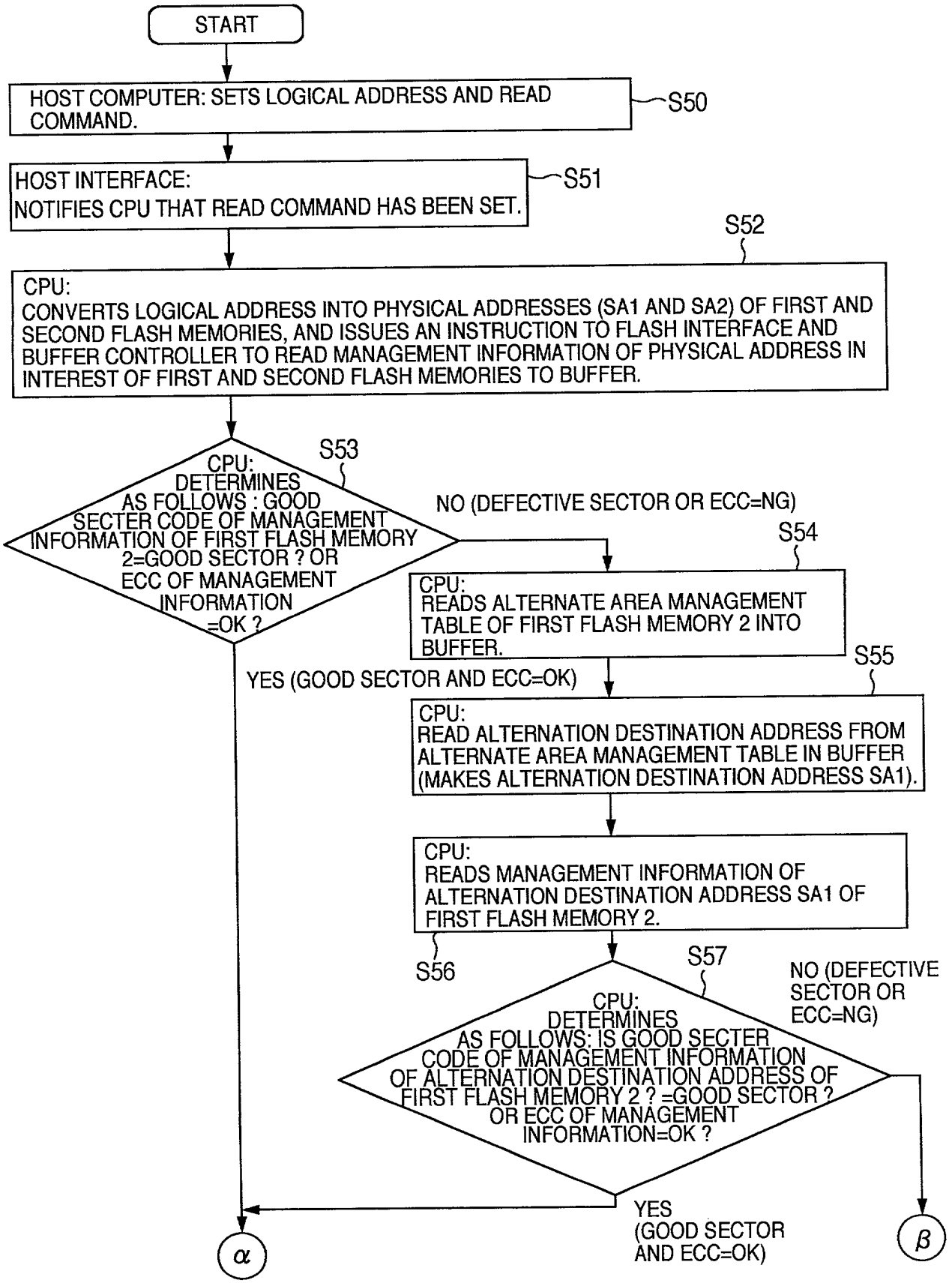
START
HOST COMPUTER: SETS LOGICAL ADDRESS AND READ COMMAND.
S50
HOST INTERFACE: NOTIFIES CPU THAT READ COMMAND HAS BEEN SET.
S51
S52
CPU: CONVERTS LOGICAL ADDRESS INTO PHYSICAL ADDRESSES (SA1 AND SA2) OF FIRST AND SECOND FLASH MEMORIES, AND ISSUES AN INSTRUCTION TO FLASH INTERFACE AND BUFFER CONTROLLER TO READ MANAGEMENT INFORMATION OF PHYSICAL ADDRESS IN INTEREST OF FIRST AND SECOND FLASH MEMORIES TO BUFFER.
S53
CPU: DETERMINES AS FOLLOWS : GOOD SECTER CODE OF MANAGEMENT INFORMATION OF FIRST FLASH MEMORY 2=GOOD SECTOR ? OR ECC OF MANAGEMENT INFORMATION =OK ?
NO (DEFECTIVE SECTOR OR ECC=NG)
S54
CPU: READS ALTERNATE AREA MANAGEMENT TABLE OF FIRST FLASH MEMORY 2 INTO BUFFER.
YES (GOOD SECTOR AND ECC=OK)
S55
CPU: READ ALTERNATION DESTINATION ADDRESS FROM ALTERNATE AREA MANAGEMENT TABLE IN BUFFER (MAKES ALTERNATION DESTINATION ADDRESS SA1).
CPU: READS MANAGEMENT INFORMATION OF ALTERNATION DESTINATION ADDRESS SA1 OF FIRST FLASH MEMORY 2.
S56
S57
CPU: DETERMINES AS FOLLOWS: IS GOOD SECTER CODE OF MANAGEMENT INFORMATION OF ALTERNATION DESTINATION ADDRESS OF FIRST FLASH MEMORY 2 ? =GOOD SECTOR ? OR ECC OF MANAGEMENT INFORMATION=OK ?
NO (DEFECTIVE SECTOR OR ECC=NG)
YES (GOOD SECTOR AND ECC=OK)
α
β

FIG.13

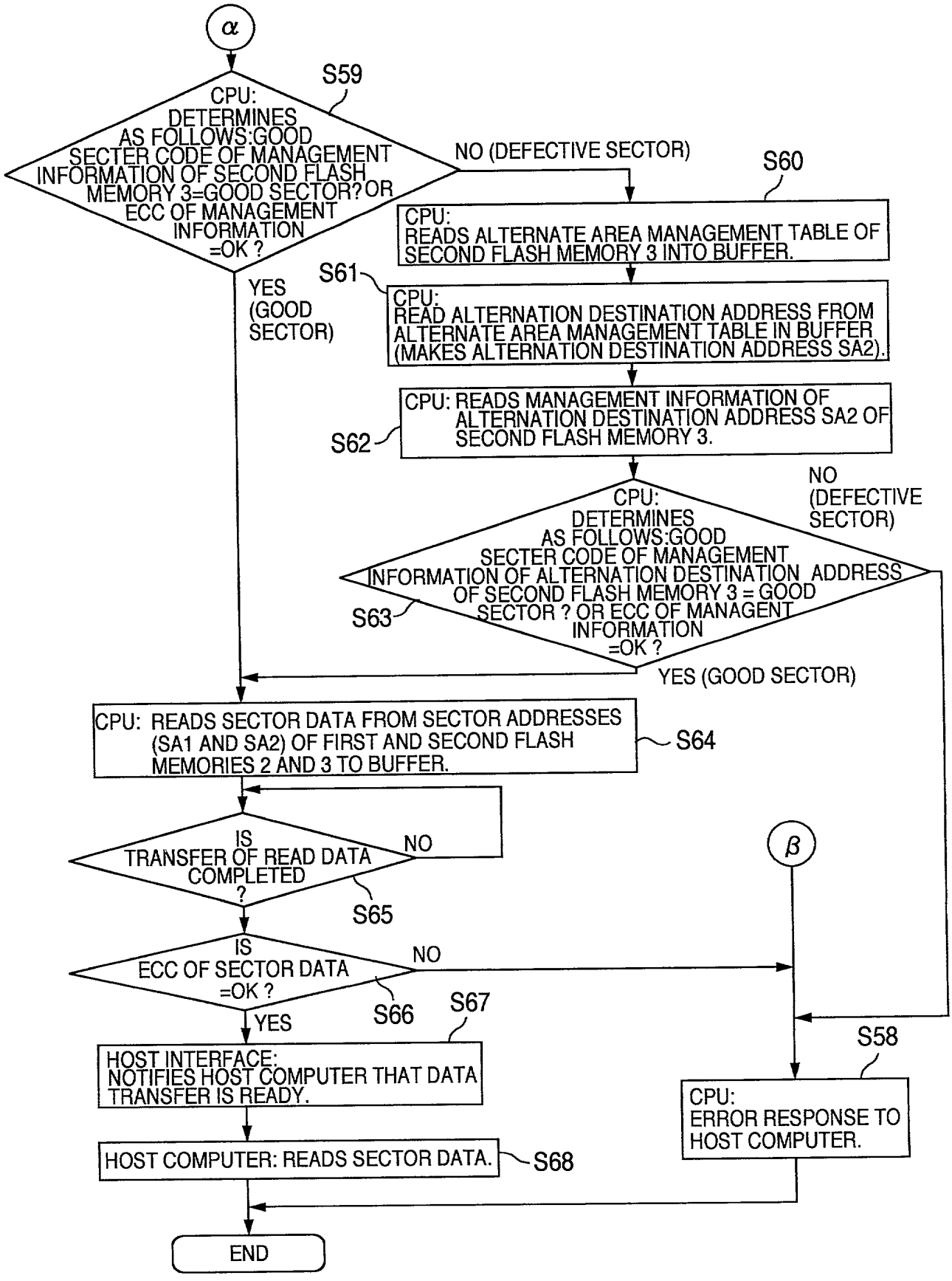
α
S59
CPU: DETERMINES AS FOLLOWS:GOOD SECTER CODE OF MANAGEMENT INFORMATION OF SECOND FLASH MEMORY 3=GOOD SECTOR? OR ECC OF MANAGEMENT INFORMATION =OK ?
NO (DEFECTIVE SECTOR)
S60
CPU: READS ALTERNATE AREA MANAGEMENT TABLE OF SECOND FLASH MEMORY 3 INTO BUFFER.
YES (GOOD SECTOR)
S61
CPU: READ ALTERNATION DESTINATION ADDRESS FROM ALTERNATE AREA MANAGEMENT TABLE IN BUFFER (MAKES ALTERNATION DESTINATION ADDRESS SA2).
CPU: READS MANAGEMENT INFORMATION OF ALTERNATION DESTINATION ADDRESS SA2 OF SECOND FLASH MEMORY 3.
S62
NO (DEFECTIVE SECTOR)
CPU: DETERMINES AS FOLLOWS:GOOD SECTER CODE OF MANAGEMENT INFORMATION OF ALTERNATION DESTINATION ADDRESS OF SECOND FLASH MEMORY 3 = GOOD SECTOR ? OR ECC OF MANAGENT INFORMATION =OK ?
S63
YES (GOOD SECTOR)
CPU: READS SECTOR DATA FROM SECTOR ADDRESSES (SA1 AND SA2) OF FIRST AND SECOND FLASH MEMORIES 2 AND 3 TO BUFFER.
S64
IS TRANSFER OF READ DATA COMPLETED ?
NO
S65
β
IS ECC OF SECTOR DATA =OK ?
NO
S66
S67
YES
HOST INTERFACE: NOTIFIES HOST COMPUTER THAT DATA TRANSFER IS READY.
S58
CPU: ERROR RESPONSE TO HOST COMPUTER.
HOST COMPUTER: READS SECTOR DATA.
S68
END

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FIG.14

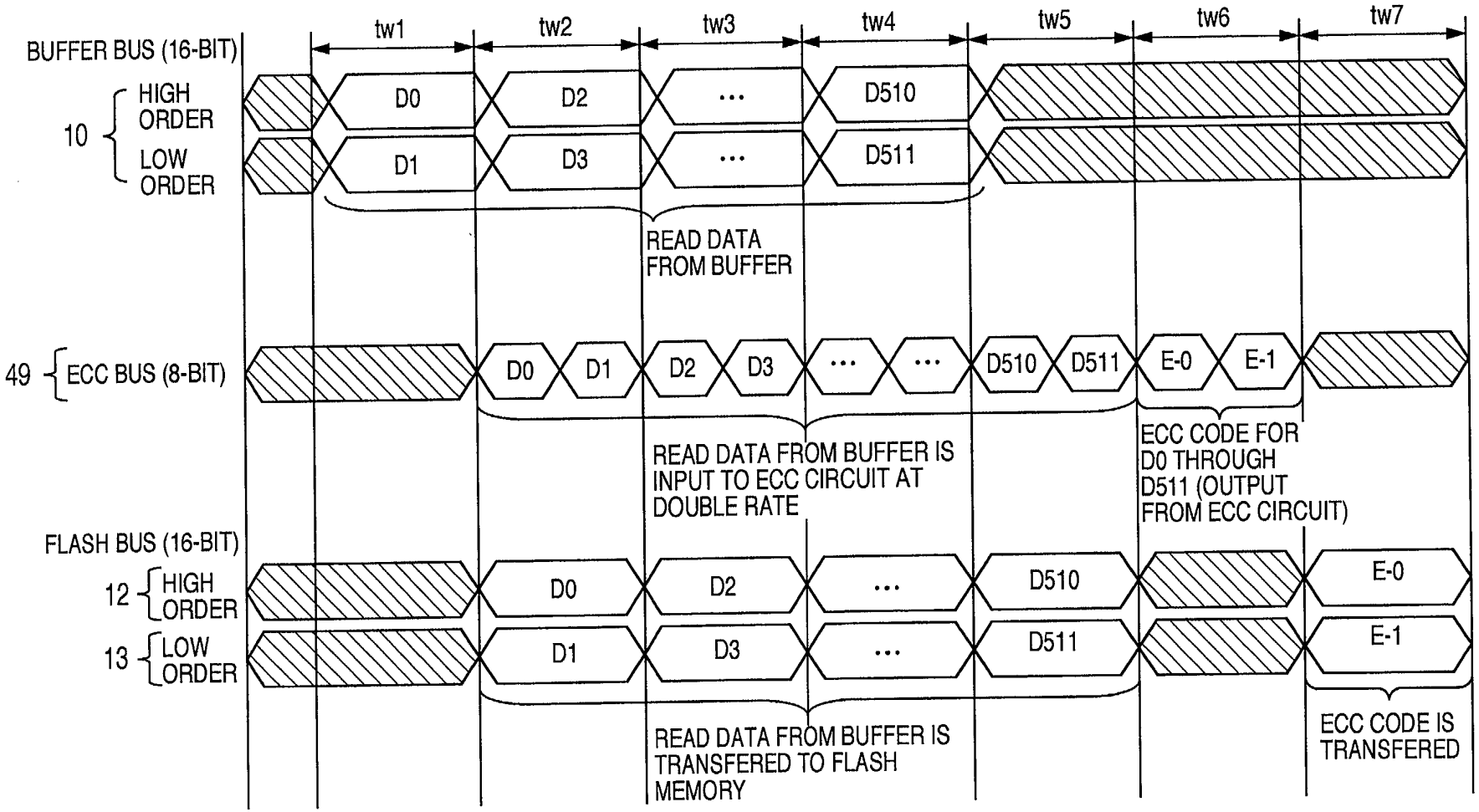


FIG.15

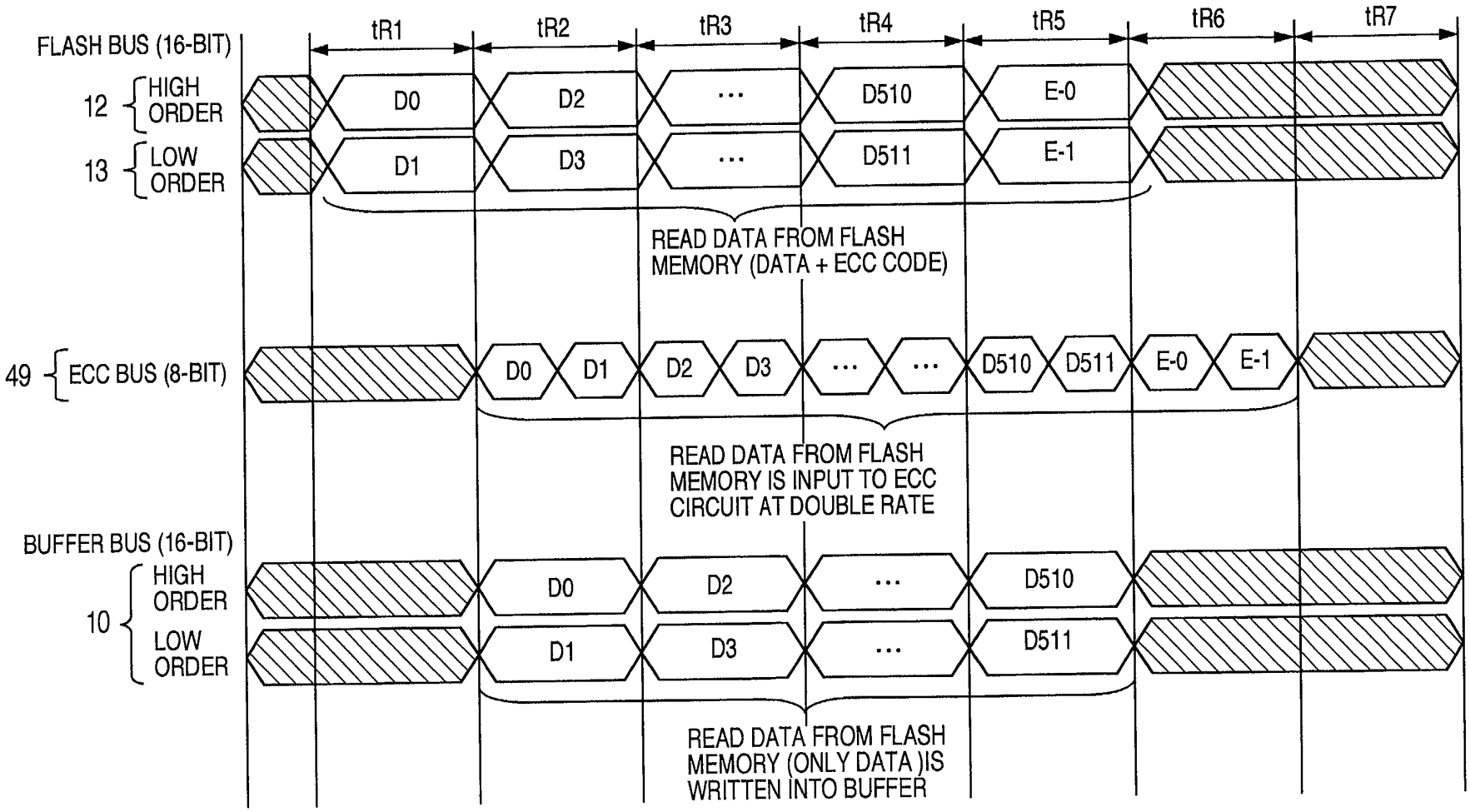

tR1
tR2
tR3
tR4
tR5
tR6
tR7
FLASH BUS (16-BIT)
12
HIGH ORDER
13
LOW ORDER
D0
D2
...
D510
E-0
D1
D3
...
D511
E-1
READ DATA FROM FLASH MEMORY (DATA + ECC CODE)
49
ECC BUS (8-BIT)
D0
D1
D2
D3
...
...
D510
D511
E-0
E-1
READ DATA FROM FLASH MEMORY IS INPUT TO ECC CIRCUIT AT DOUBLE RATE
BUFFER BUS (16-BIT)
10
HIGH ORDER
LOW ORDER
D0
D2
...
D510
D1
D3
...
D511
READ DATA FROM FLASH MEMORY (ONLY DATA)IS WRITTEN INTO BUFFER

FIG.16

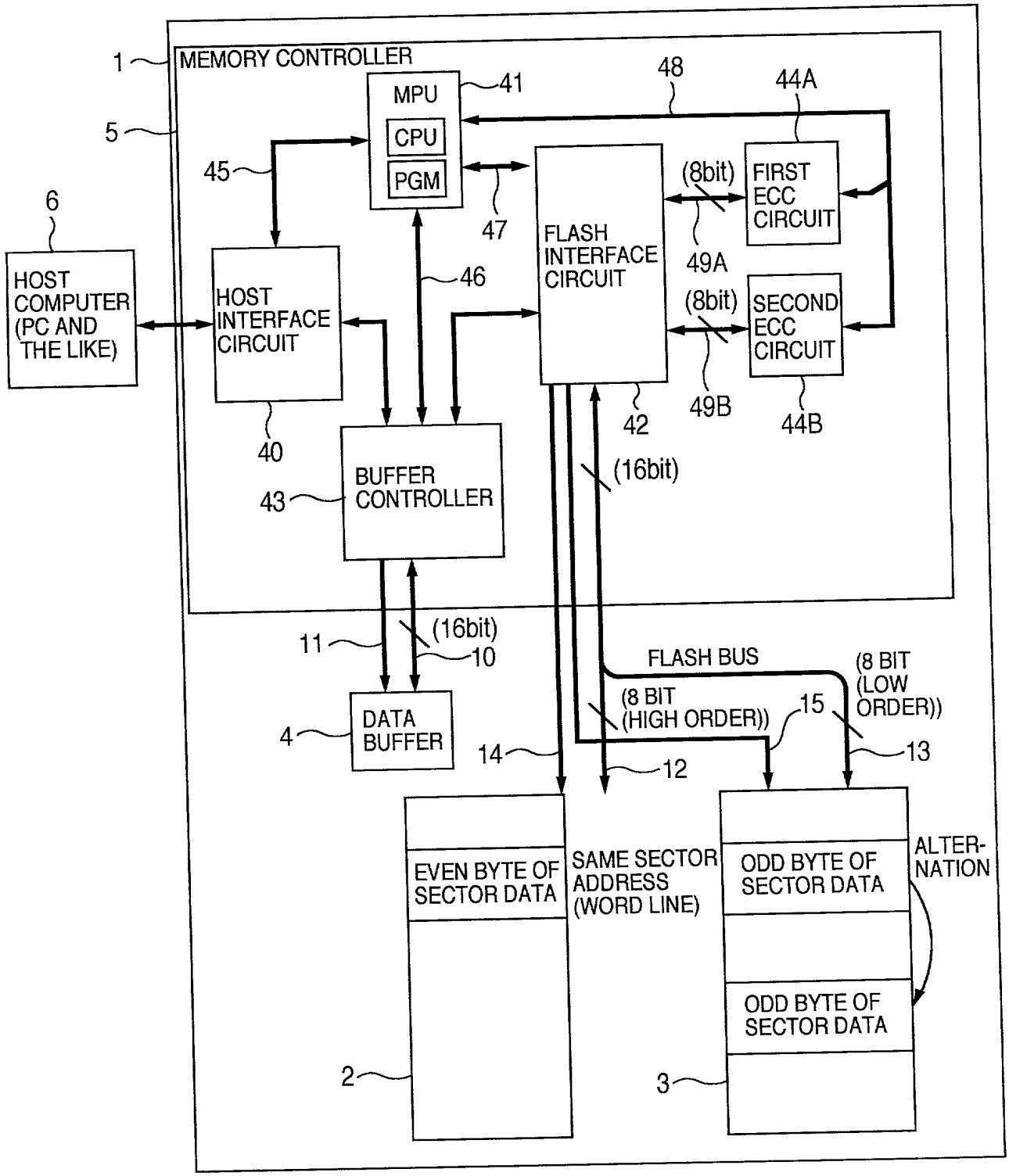

1
MEMORY CONTROLLER
MPU
41
CPU
PGM
48
44A
5
45
47
6
HOST COMPUTER (PC AND THE LIKE)
HOST INTERFACE CIRCUIT
46
FLASH INTERFACE CIRCUIT
(8bit)
FIRST ECC CIRCUIT
49A
(8bit)
SECOND ECC CIRCUIT
49B
44B
42
40
BUFFER CONTROLLER
43
(16bit)
11
(16bit)
10
FLASH BUS
(8 BIT (LOW ORDER))
(8 BIT (HIGH ORDER))
15
4
DATA BUFFER
14
12
13
EVEN BYTE OF SECTOR DATA
SAME SECTOR ADDRESS (WORD LINE)
ODD BYTE OF SECTOR DATA
ALTER-NATION
ODD BYTE OF SECTOR DATA
2
3

FIG.17

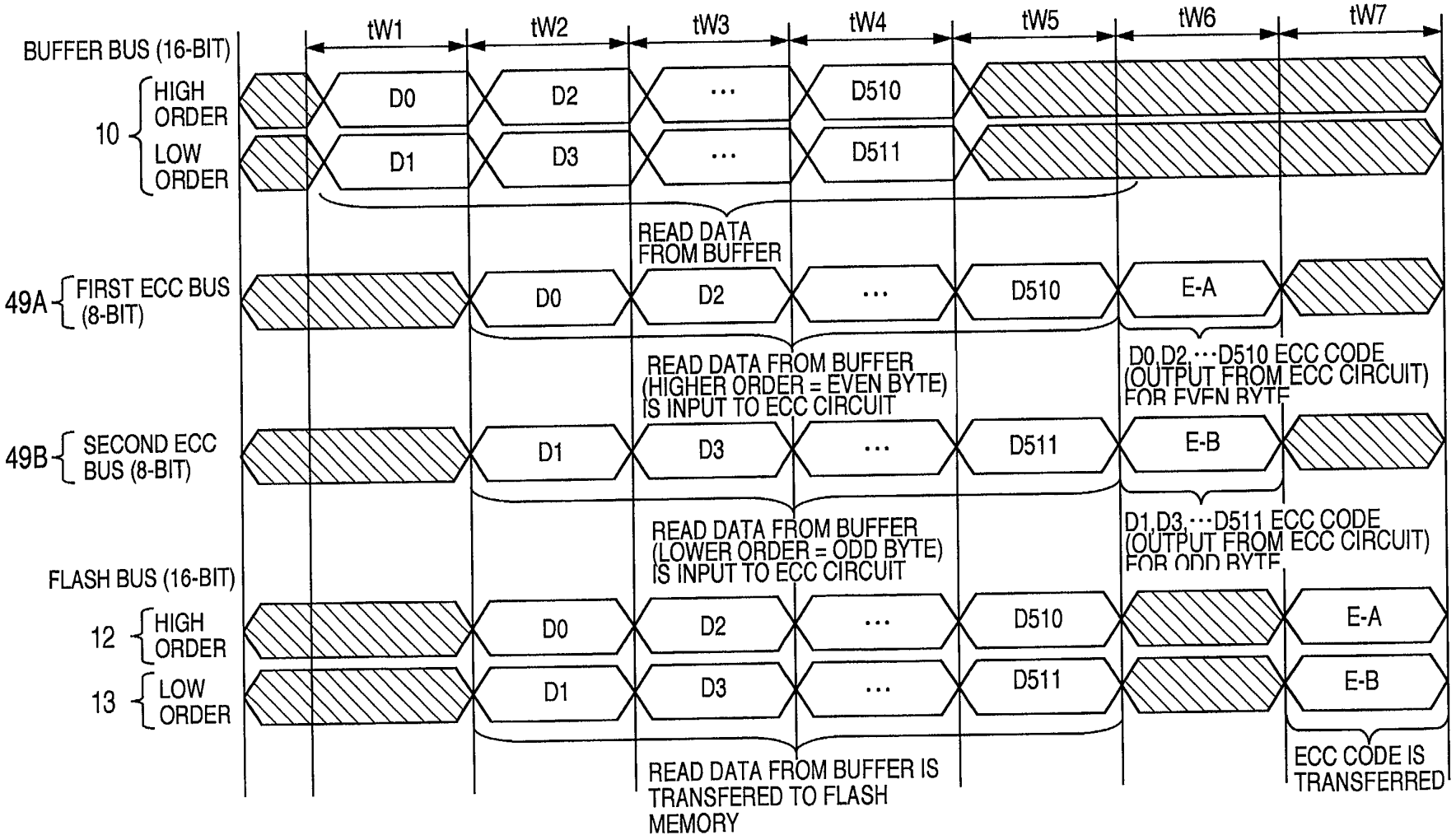

tW1
tW2
tW3
tW4
tW5
tW6
tW7
BUFFER BUS (16-BIT)
10
HIGH ORDER
LOW ORDER
D0
D2
D510
D1
D3
D511
READ DATA FROM BUFFER
49A
FIRST ECC BUS (8-BIT)
E-A
READ DATA FROM BUFFER (HIGHER ORDER = EVEN BYTE) IS INPUT TO ECC CIRCUIT
D0,D2,···D510 ECC CODE (OUTPUT FROM ECC CIRCUIT) FOR EVEN BYTE
49B
SECOND ECC BUS (8-BIT)
E-B
READ DATA FROM BUFFER (LOWER ORDER = ODD BYTE) IS INPUT TO ECC CIRCUIT
D1,D3,···D511 ECC CODE (OUTPUT FROM ECC CIRCUIT) FOR ODD BYTE
FLASH BUS (16-BIT)
12
13
READ DATA FROM BUFFER IS TRANSFERED TO FLASH MEMORY
ECC CODE IS TRANSFERRED

FIG.18

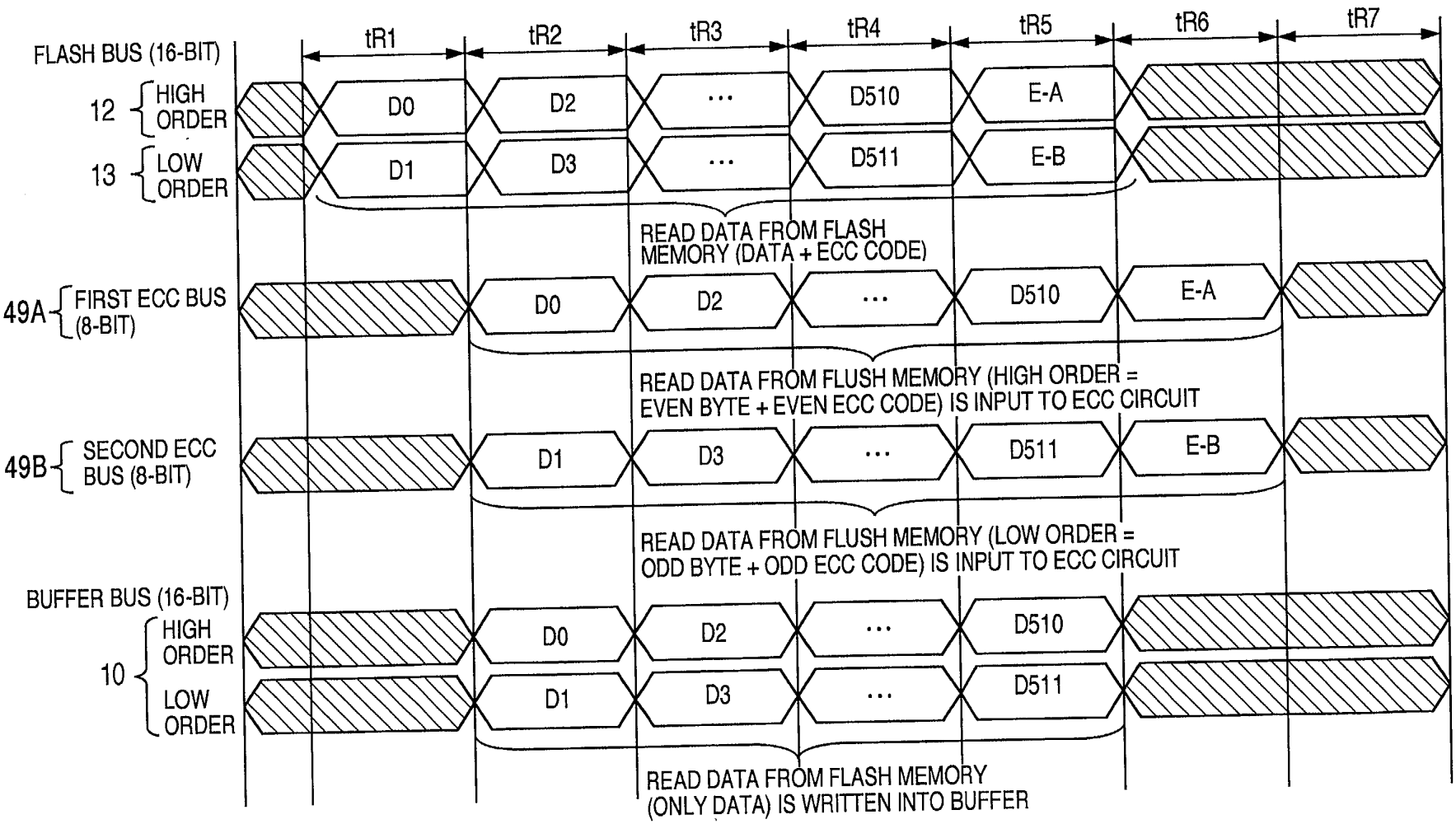

tR1
tR2
tR3
tR4
tR5
tR6
tR7
FLASH BUS (16-BIT)
12 HIGH ORDER
13 LOW ORDER
D0
D2
...
D510
E-A
D1
D3
...
D511
E-B
READ DATA FROM FLASH MEMORY (DATA + ECC CODE)
49A FIRST ECC BUS (8-BIT)
D0
D2
...
D510
E-A
READ DATA FROM FLUSH MEMORY (HIGH ORDER = EVEN BYTE + EVEN ECC CODE) IS INPUT TO ECC CIRCUIT
49B SECOND ECC BUS (8-BIT)
D1
D3
...
D511
E-B
READ DATA FROM FLUSH MEMORY (LOW ORDER = ODD BYTE + ODD ECC CODE) IS INPUT TO ECC CIRCUIT
BUFFER BUS (16-BIT)
10 HIGH ORDER
LOW ORDER
D0
D2
...
D510
D1
D3
...
D511
READ DATA FROM FLASH MEMORY (ONLY DATA) IS WRITTEN INTO BUFFER

FIG.19

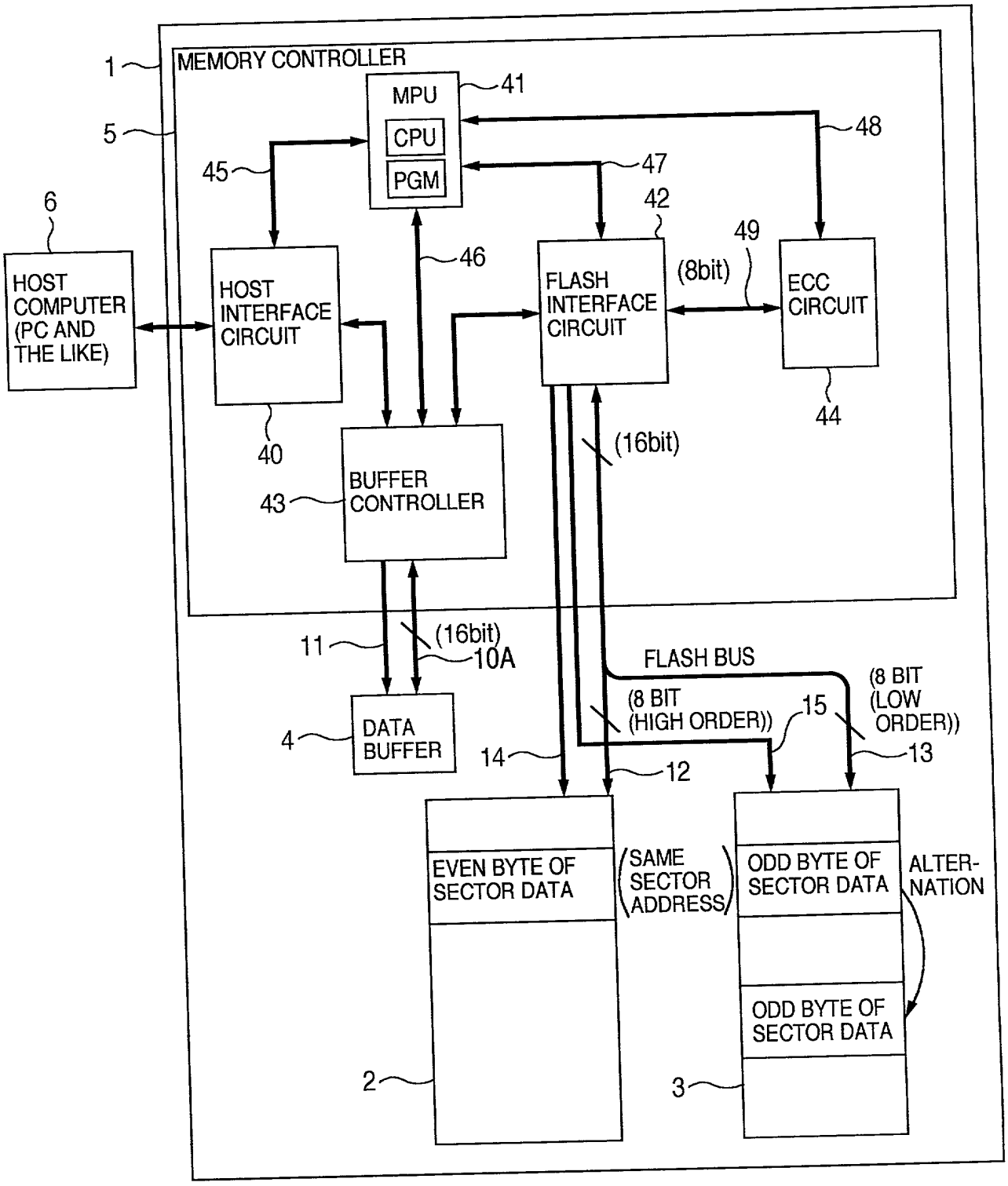

MEMORY CONTROLLER
1
MPU
41
CPU
PGM
5
45
47
48
42
49
6
HOST COMPUTER (PC AND THE LIKE)
HOST INTERFACE CIRCUIT
46
FLASH INTERFACE CIRCUIT
(8bit)
ECC CIRCUIT
44
40
BUFFER CONTROLLER
43
(16bit)
11
(16bit)
10A
FLASH BUS
(8 BIT (HIGH ORDER))
15
(8 BIT (LOW ORDER))
4
DATA BUFFER
14
12
13
EVEN BYTE OF SECTOR DATA
(SAME SECTOR ADDRESS)
ODD BYTE OF SECTOR DATA
ALTER-NATION
ODD BYTE OF SECTOR DATA
2
3

FIG.20

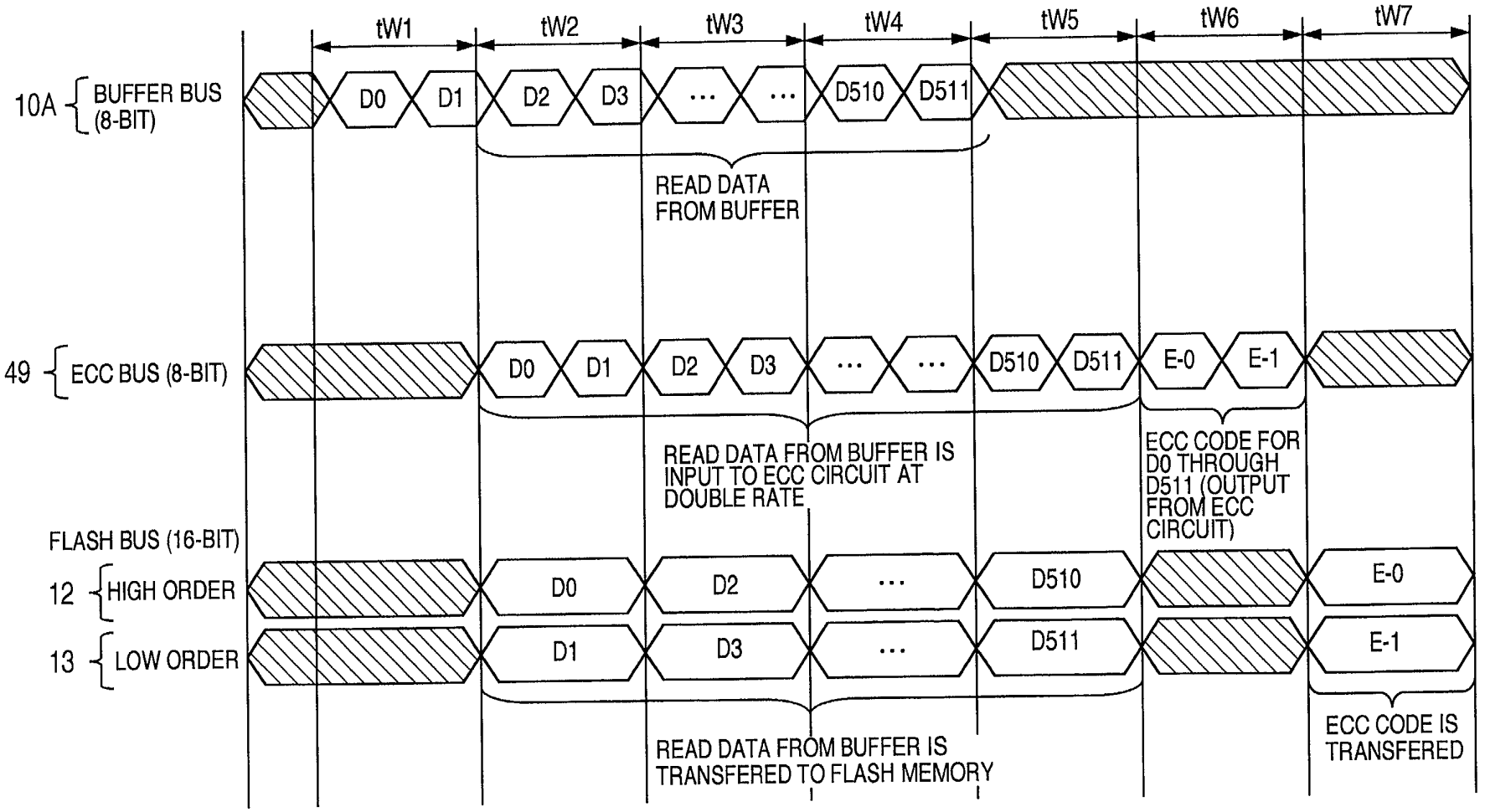
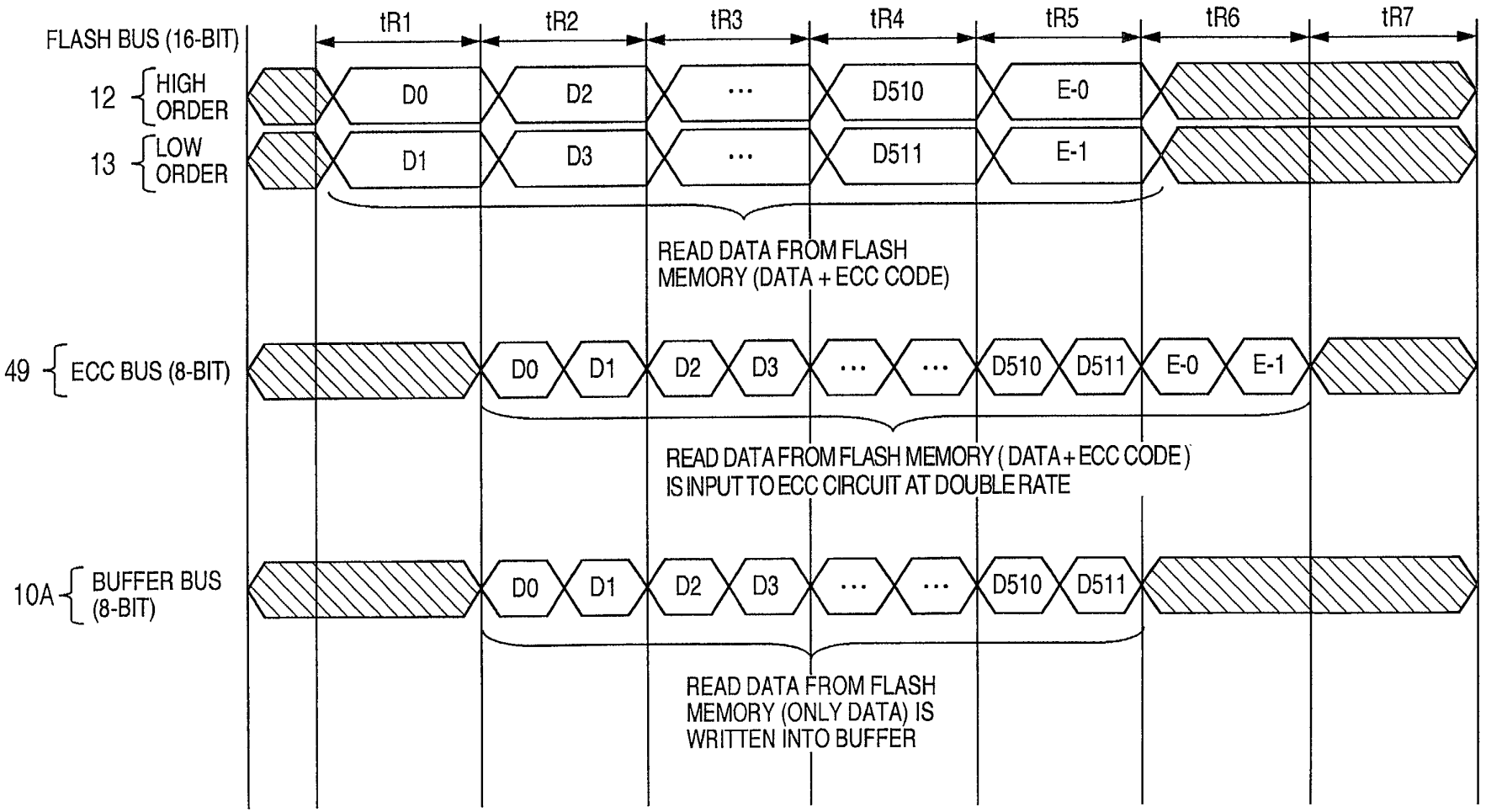

tW1
tW2
tW3
tW4
tW5
tW6
tW7
10A
BUFFER BUS (8-BIT)
D0
D1
D2
D3
D510
D511
READ DATA FROM BUFFER
49
ECC BUS (8-BIT)
E-0
E-1
READ DATA FROM BUFFER IS INPUT TO ECC CIRCUIT AT DOUBLE RATE
ECC CODE FOR D0 THROUGH D511 (OUTPUT FROM ECC CIRCUIT)
FLASH BUS (16-BIT)
12
HIGH ORDER
13
LOW ORDER
READ DATA FROM BUFFER IS TRANSFERED TO FLASH MEMORY
ECC CODE IS TRANSFERED

FIG.21


FLASH BUS (16-BIT)
12 HIGH ORDER
13 LOW ORDER
tR1
tR2
tR3
tR4
tR5
tR6
tR7
D0
D2
...
D510
E-0
D1
D3
...
D511
E-1
READ DATA FROM FLASH MEMORY (DATA + ECC CODE)
49 ECC BUS (8-BIT)
D0
D1
D2
D3
...
...
D510
D511
E-0
E-1
READ DATA FROM FLASH MEMORY (DATA + ECC CODE) IS INPUT TO ECC CIRCUIT AT DOUBLE RATE
10A BUFFER BUS (8-BIT)
D0
D1
D2
D3
...
...
D510
D511
READ DATA FROM FLASH MEMORY (ONLY DATA) IS WRITTEN INTO BUFFER